

PG166-A02

TU116,192b GDDR6 2CHx16,90W/120W DVI-D DL + HDMI + DP

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Page Description

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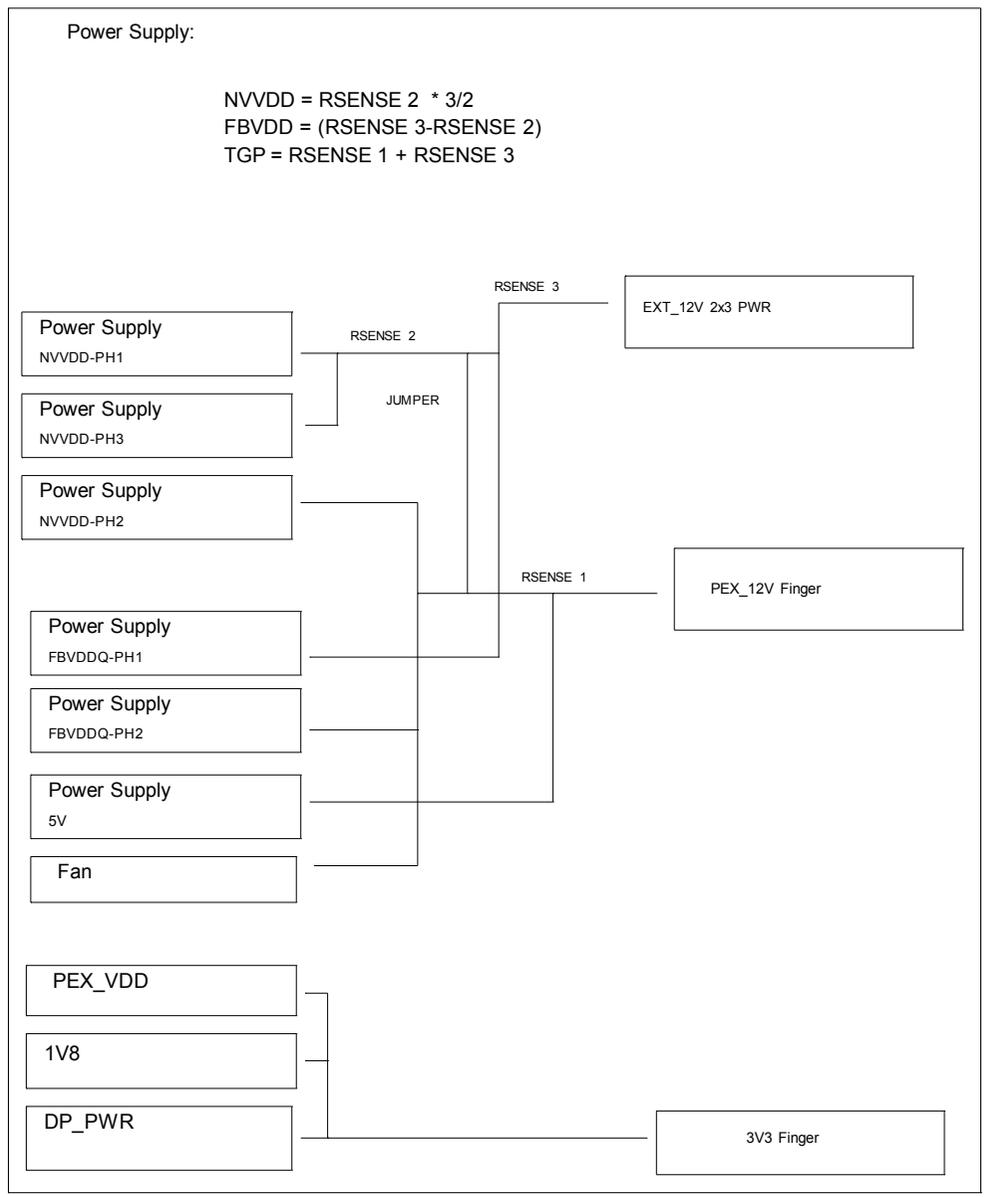
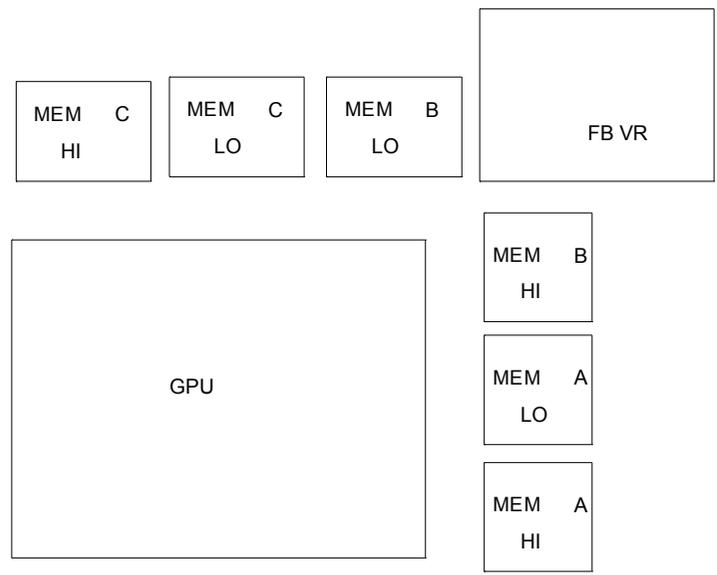
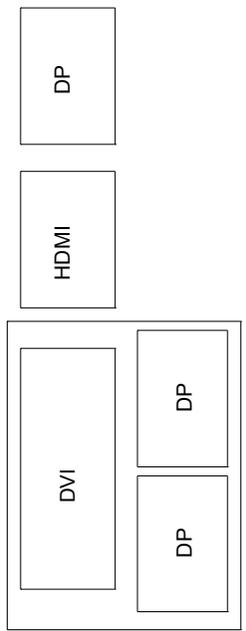
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ASSEMBLY	ASSEMBLY DESCRIPTION
FRGE DETAIL	Table of Contents

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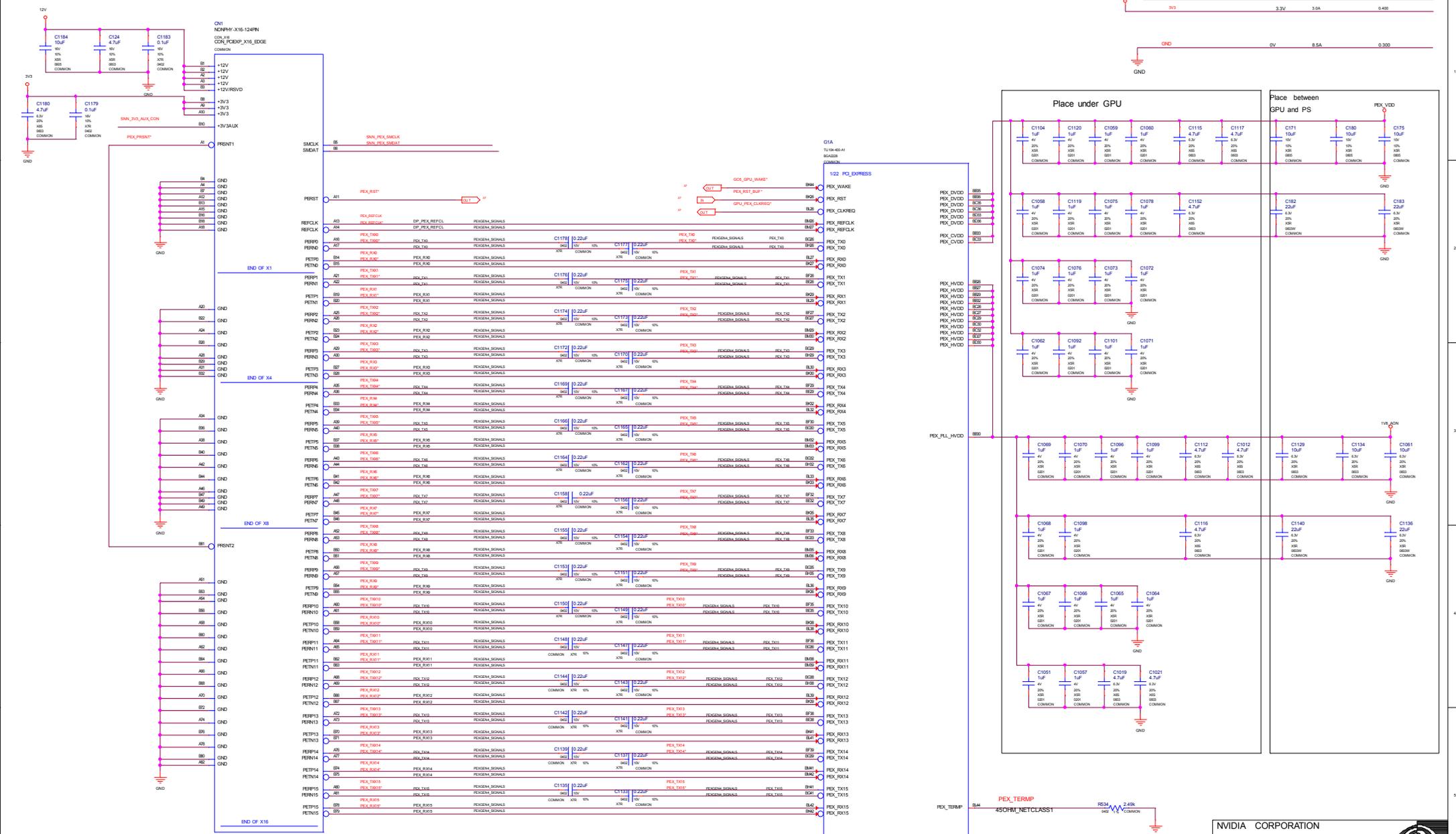


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ASSEMBLY	ASSEMBLY DESCRIPTION
PCB DETAIL	Block Diagram

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NV_PN	600-1G166-BASE-A02	PRG#	2 OF 4T
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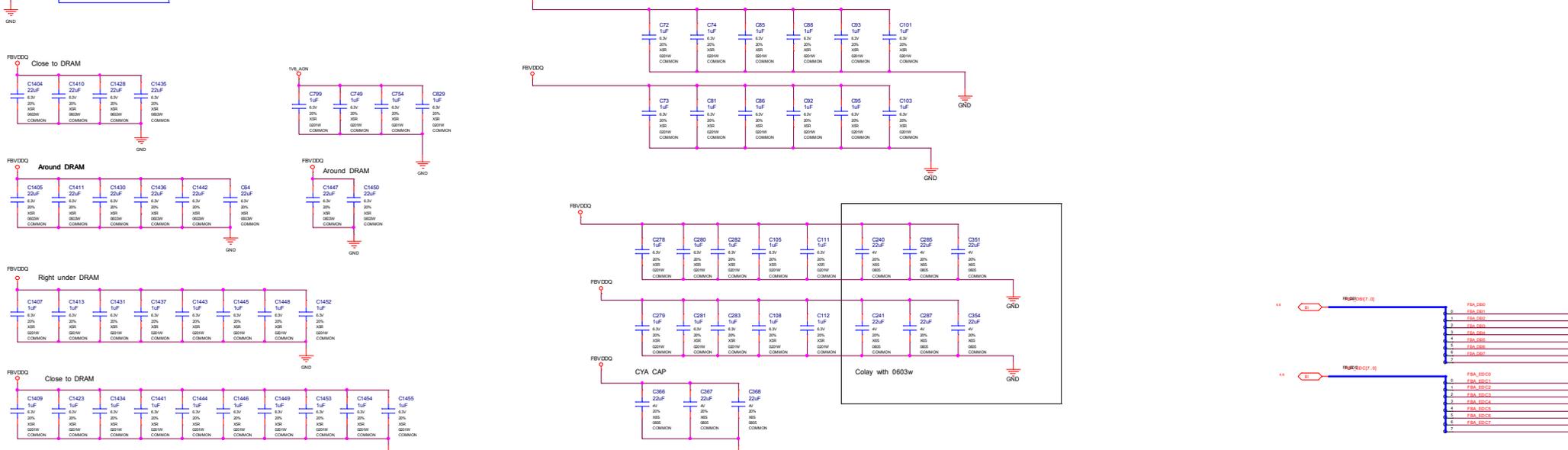
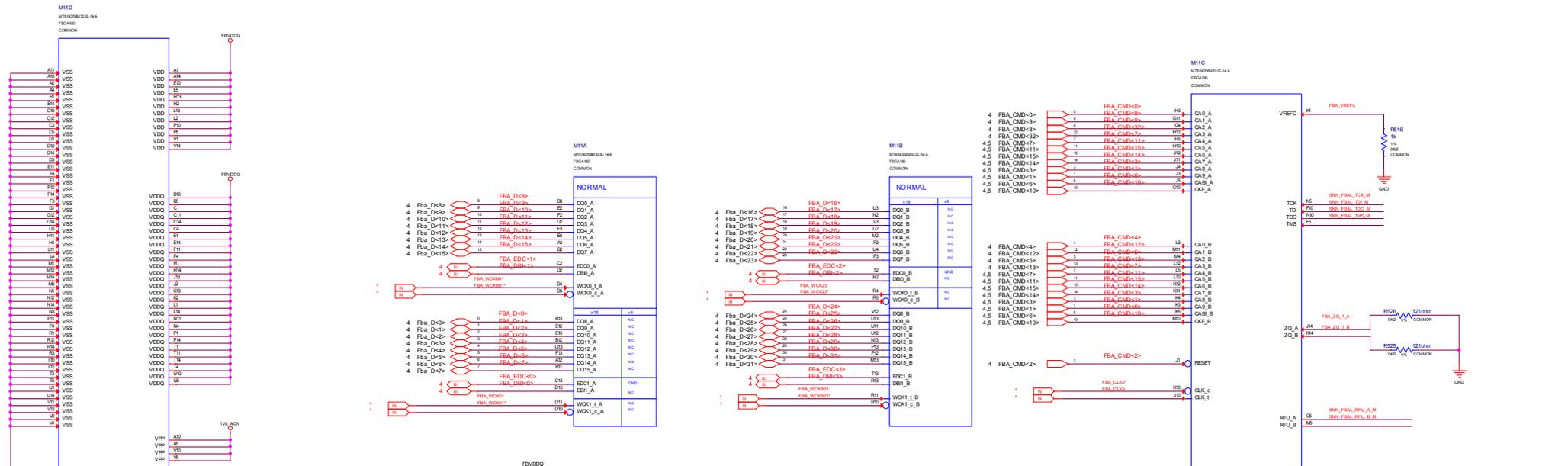
VOLTAJE	MAX_CURRENT	MIN_WIDTH
12V	5.5A	0.450
5V	3.0A	0.450
3.3V	3.0A	0.450

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ASSEMBLY PART DESCRIPTION	PCI Express
PCB REV	10166-A02
PCB REV	A
DATE	01-AUG-2019

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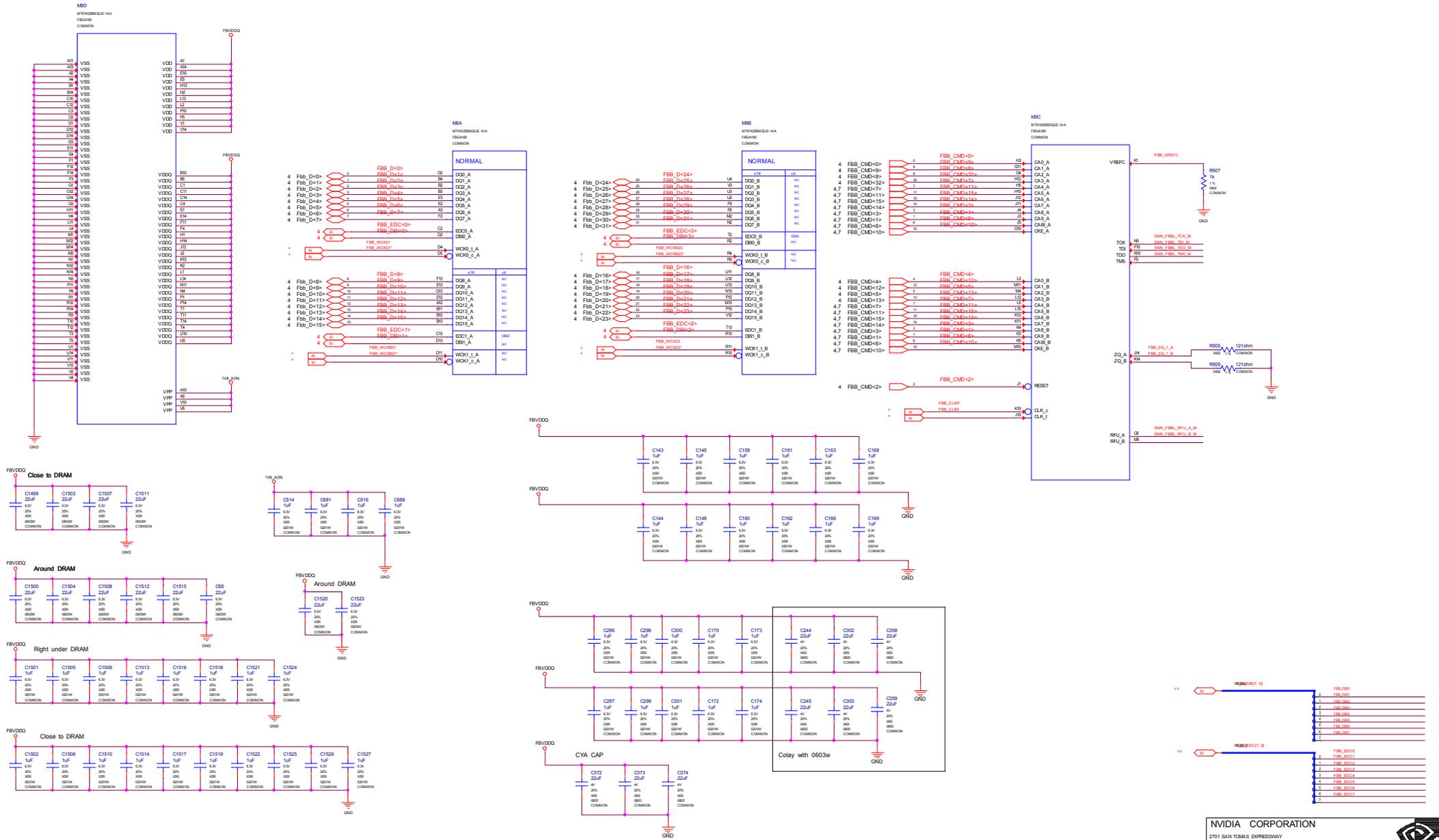


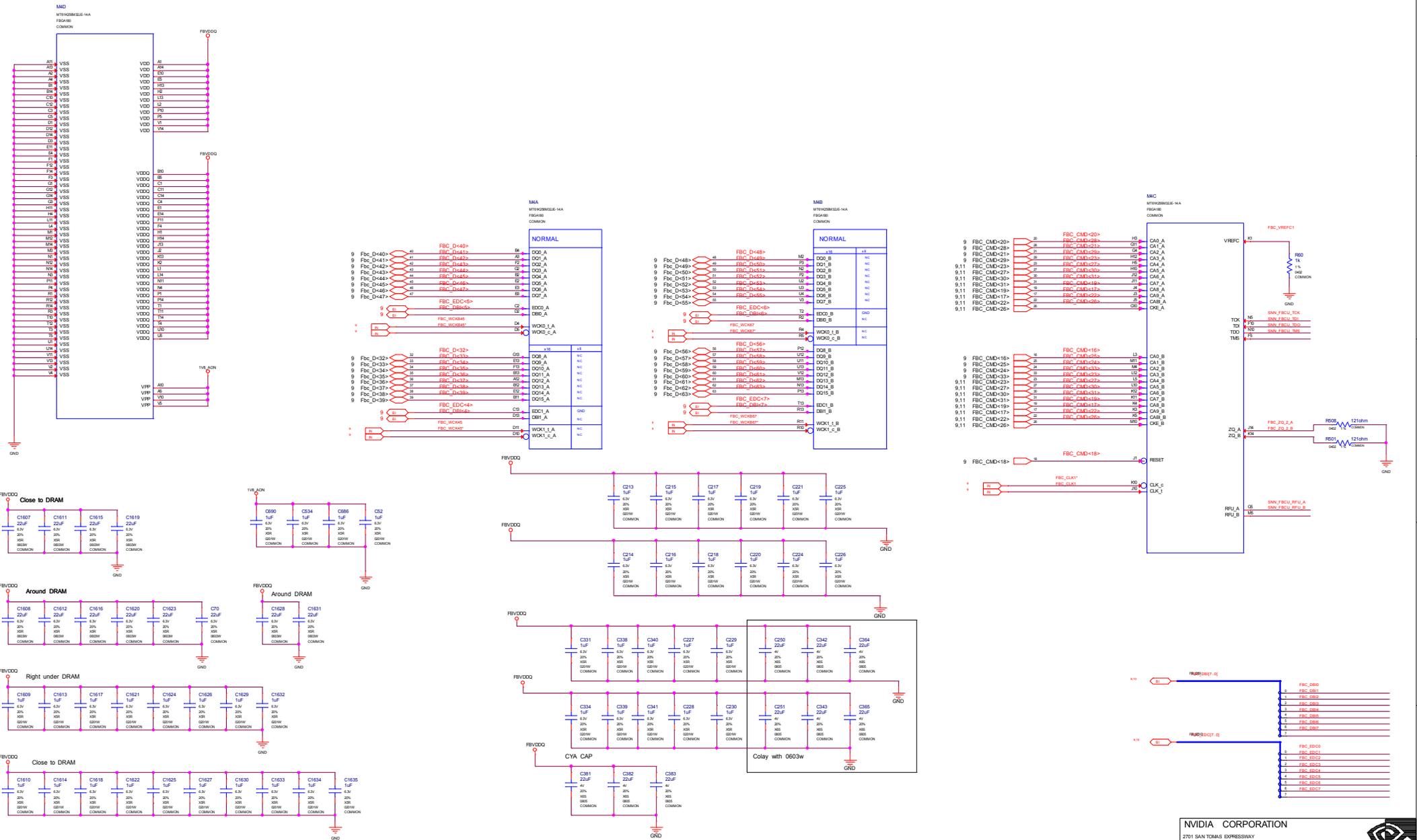
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PAGE DETAIL	MEMORY: FBA[110]		

NV_PN		600-1G166-BASE-A02	
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BCM REV	A	DATE	01-AUG-2019

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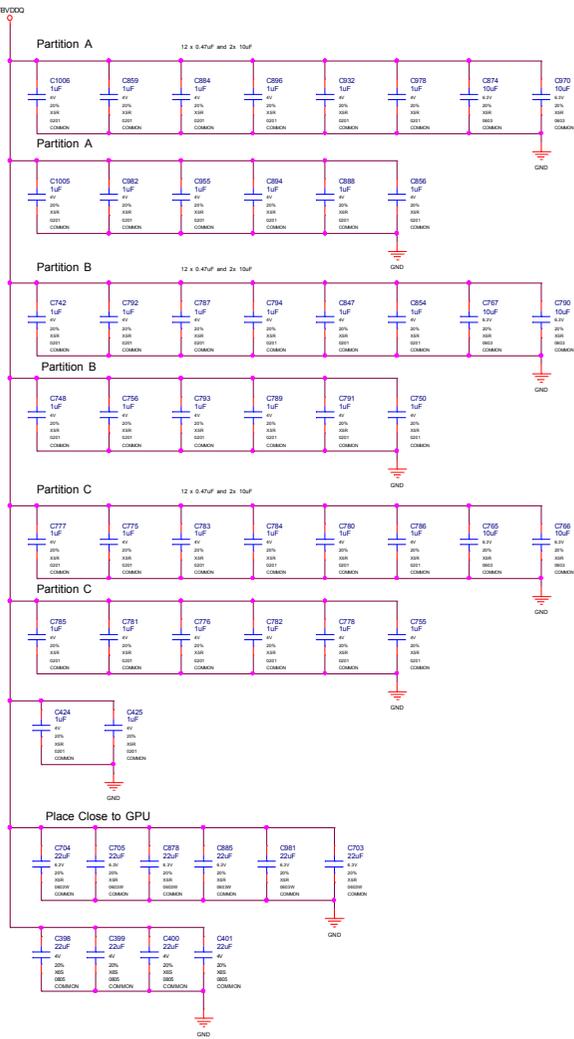
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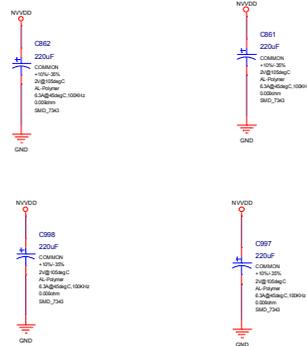
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 BCM REV A DATE 01.AUG.2019

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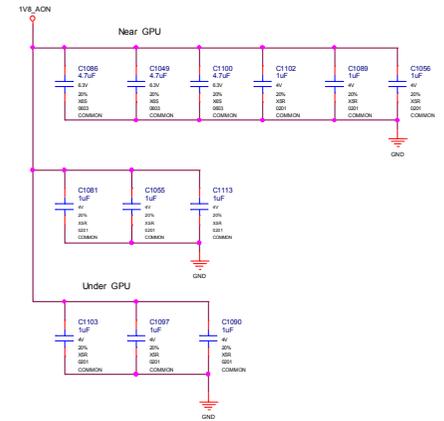
FBVDDQ



NVDD



1V8_AON

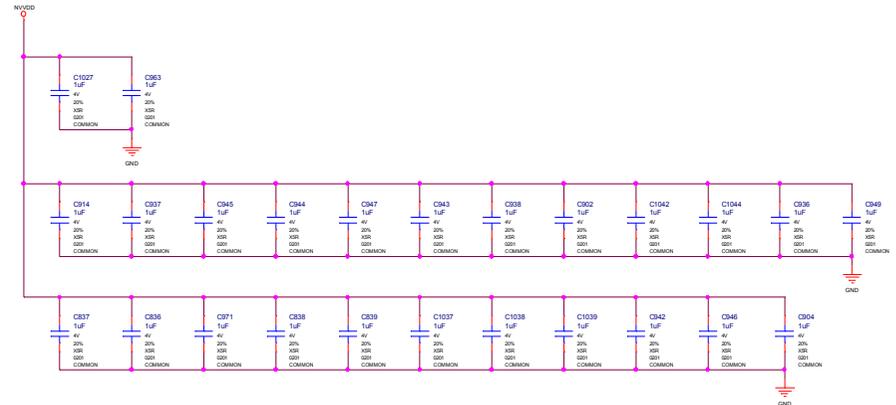
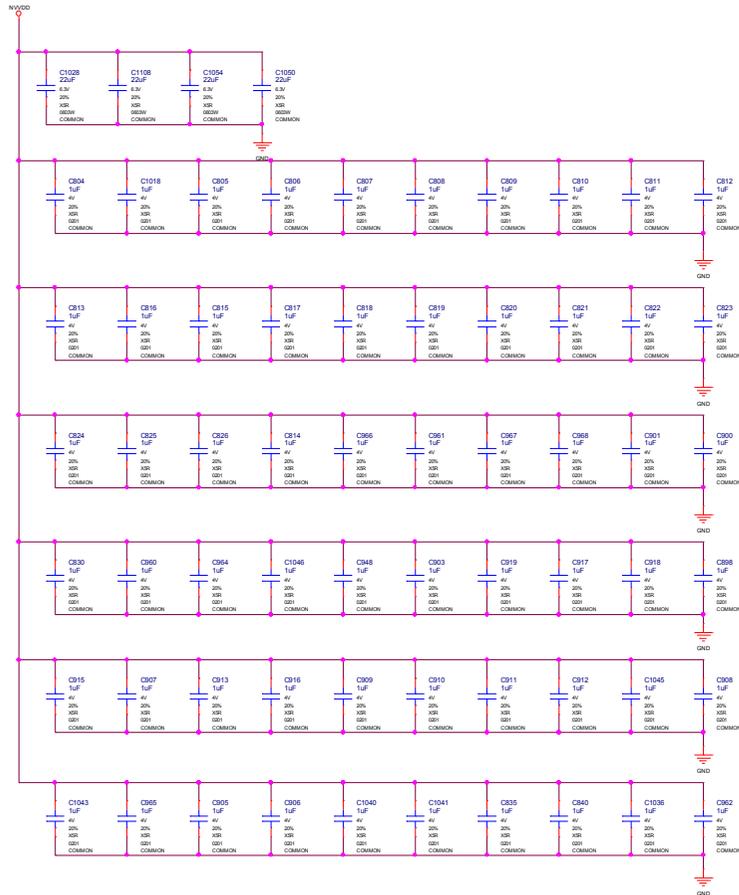


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ASSEMBLY	ASSEMBLY DESCRIPTION
FRGE DETAIL	GPU DECOUPLING 1

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NVDD

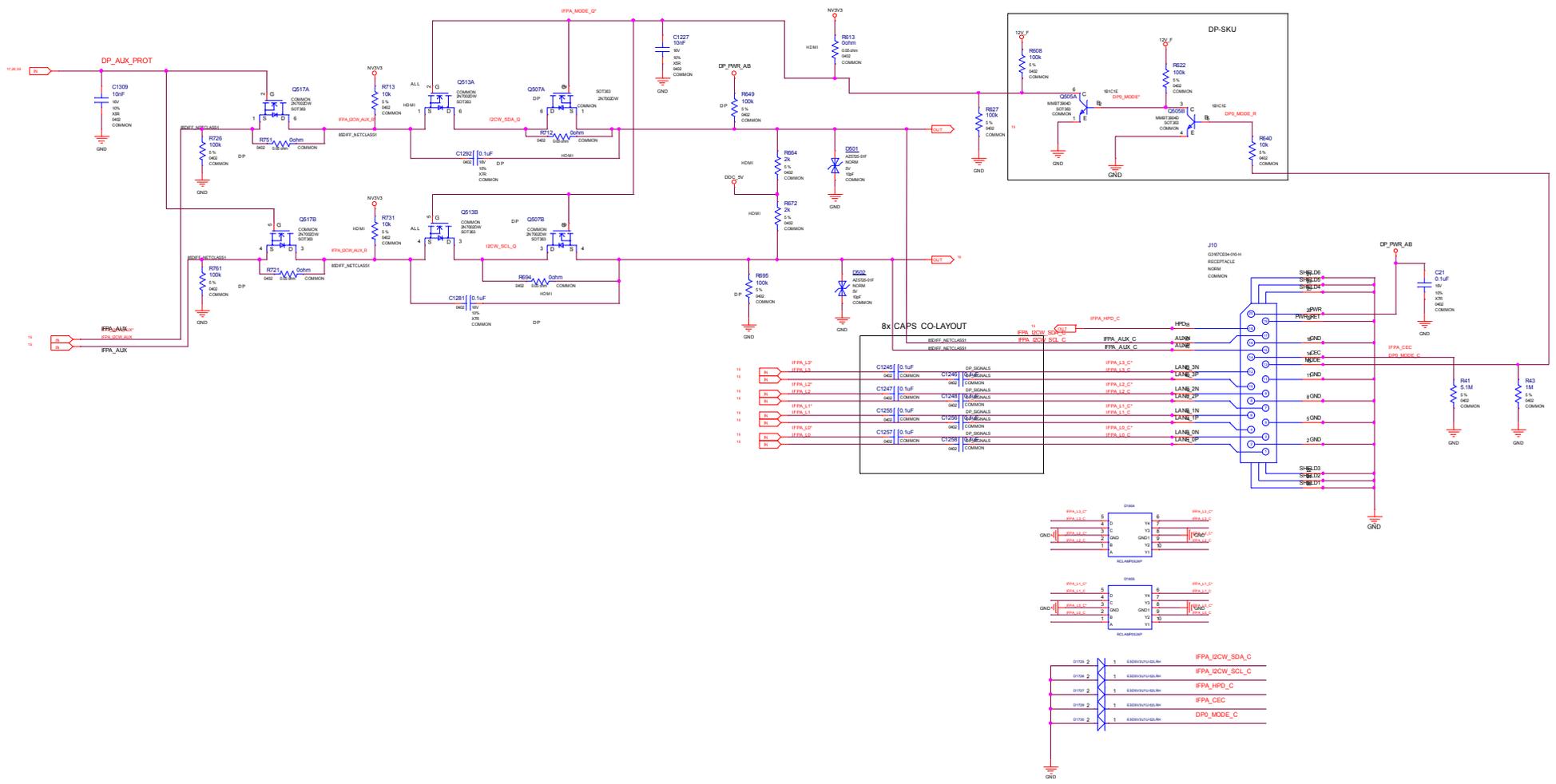


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ASSEMBLY	<ASSEMBLY_DESCRIPTION>
FIGURE DETAIL	GPU DECOUPLING 2

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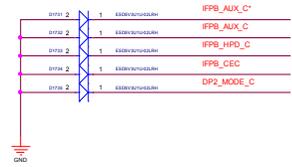
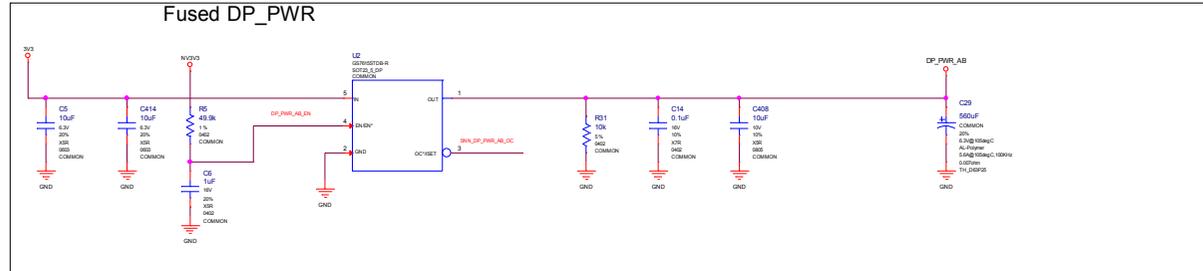
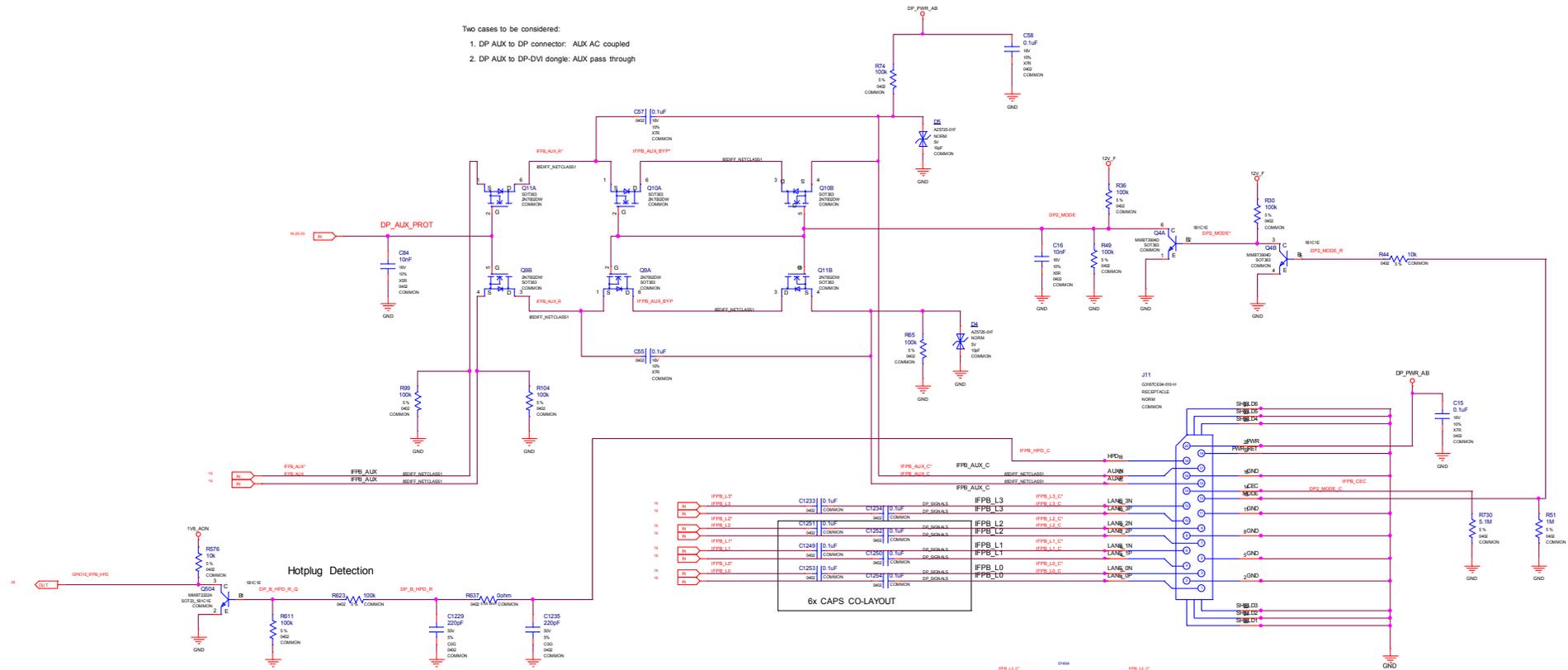
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NV_PN: **600-1G166-BASE-A02**

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Two cases to be considered:
 1. DP AUX to DP connector: AUX AC coupled
 2. DP AUX to DP-DVI dongle: AUX pass through



ASSEMBLY DESCRIPTION
 IC: IFPB DP

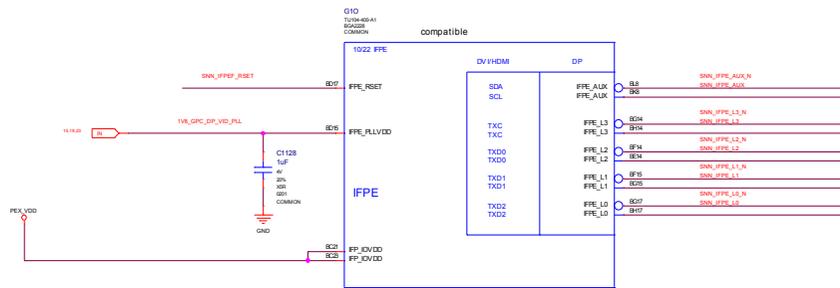
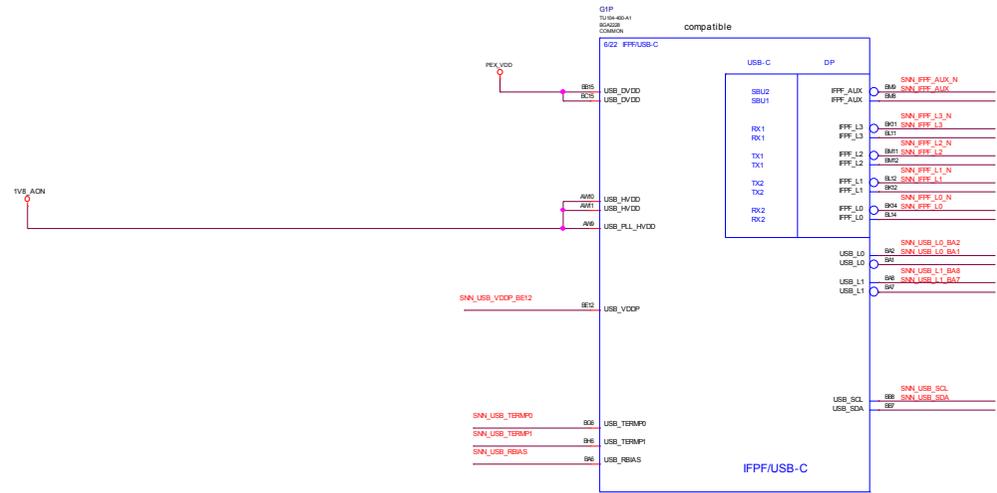
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Nv_PN 600-1G166-BASE-A02A
 PCB REV TGT166-A02
 BOM REV A

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 DATE 01-AUG-2019





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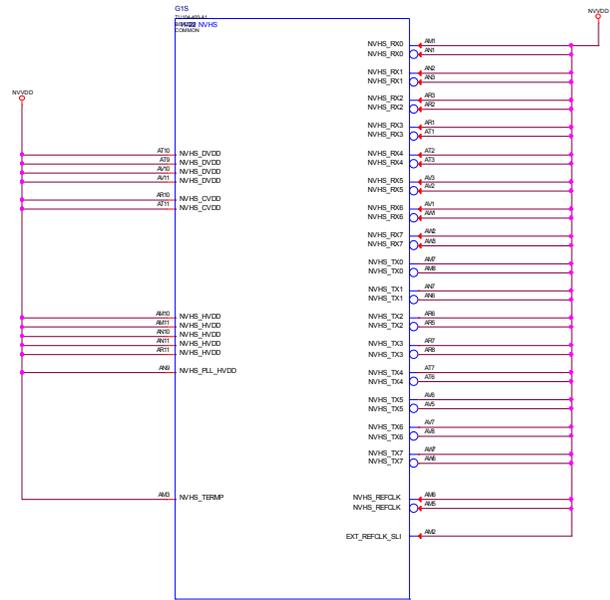
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PAGE DETAIL	

ID: IFPE & IFPF NC

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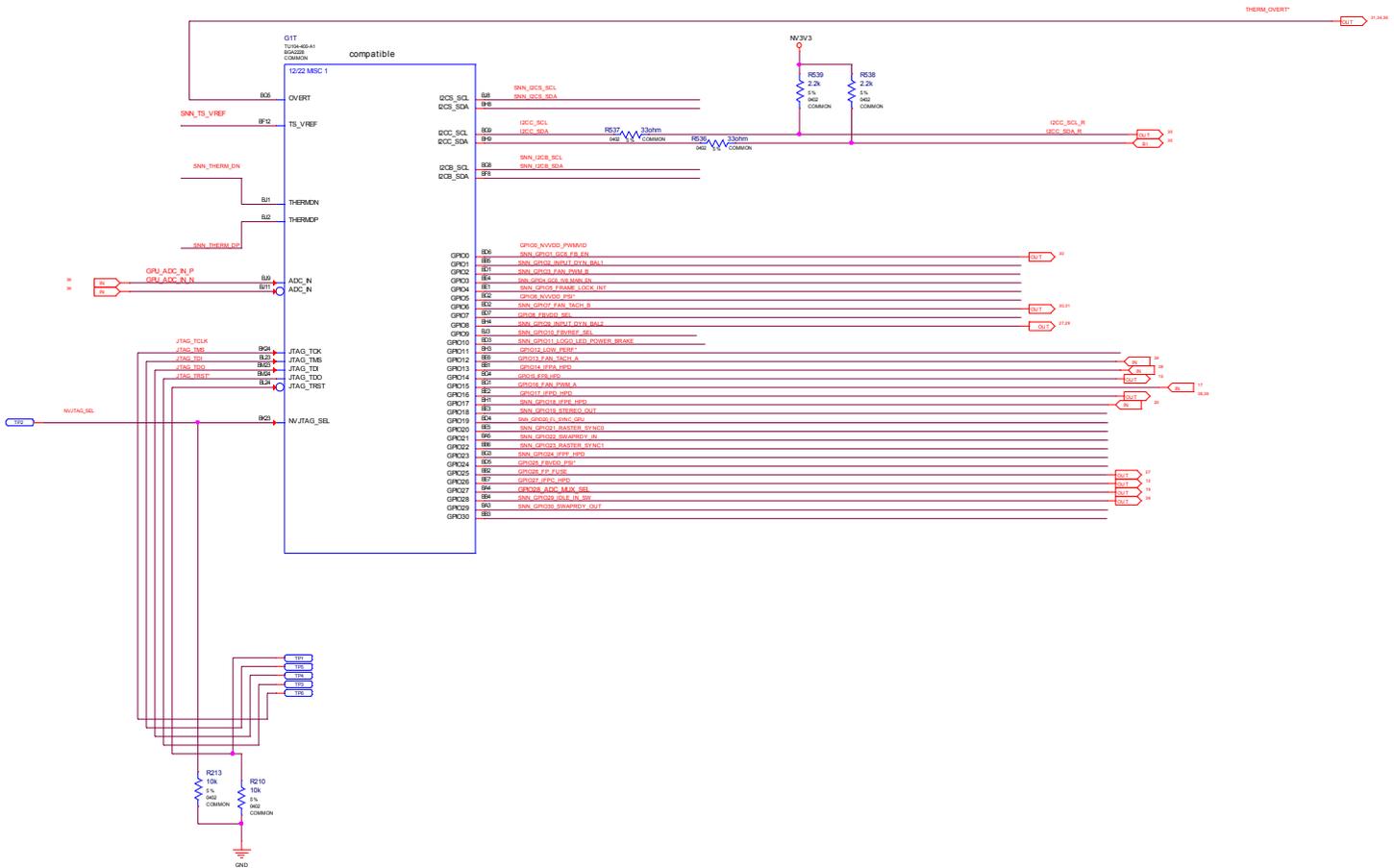
Use NC pin to Improve NVVDD,FBVDDQ,1V8 PDN
For TU116 Only



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ASSEMBLY	ASSEMBLY DESCRIPTION
FRGE DETAIL	ID: NVHS INTERFACE AND FRAME LOCK



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ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	MISC1: JTAG,GPIO,ADC,I2C,OVERT

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STRAP2	STRAP1	STRAP0	RAMCFG[4:0]
L	L	L	00000
L	L	H	00001
L	H	L	00010
L	H	H	00011
H	H	L	00110
H	H	H	00111
L	L	M	01000

STRAP2	STRAP1	STRAP0	RAMCFG[4:0]	
L	L	L	0000	Samsung 8Gb 256Mx32 K4Z80325BC-HC14
L	L	H	0001	Micron 8Gb 256Mx32 MT61K256M32JE-14-A
L	H	L	0010	Hynix 8Gb 256Mx32 H56C8H24MJR-S2C
L	H	H	0011	Samsung 8Gb 256Mx32 K4Z8032BC-HC12
H	H	L	0110	
H	H	H	0111	
L	L	M	1000	
L	L	L	1001	

ROM_SO	ROM_SI	ROM_SCLK	DUMMY[2:0].FS_OVERT	1.ENABLE 0.DISABLE	
L	L	L	XXX1	FS_OVERT ENABLE	DEFAULT
L	L	M	XXX0	FS_OVERT DISABLE	

STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
M	H	H	1	1	1	1
M	H	L	1	1	1	0
M	L	H	1	1	0	1
M	L	L	1	1	0	0
L	H	M	1	0	1	1
L	M	L	1	0	0	1
L	L	M	1	0	0	0
H	H	H	0	1	1	1
H	H	L	0	1	1	0
H	L	H	0	1	0	1
H	L	L	0	1	0	0
L	H	H	0	0	1	1
L	H	L	0	0	1	0
L	L	H	0	0	0	1
L	L	L	0	0	0	0

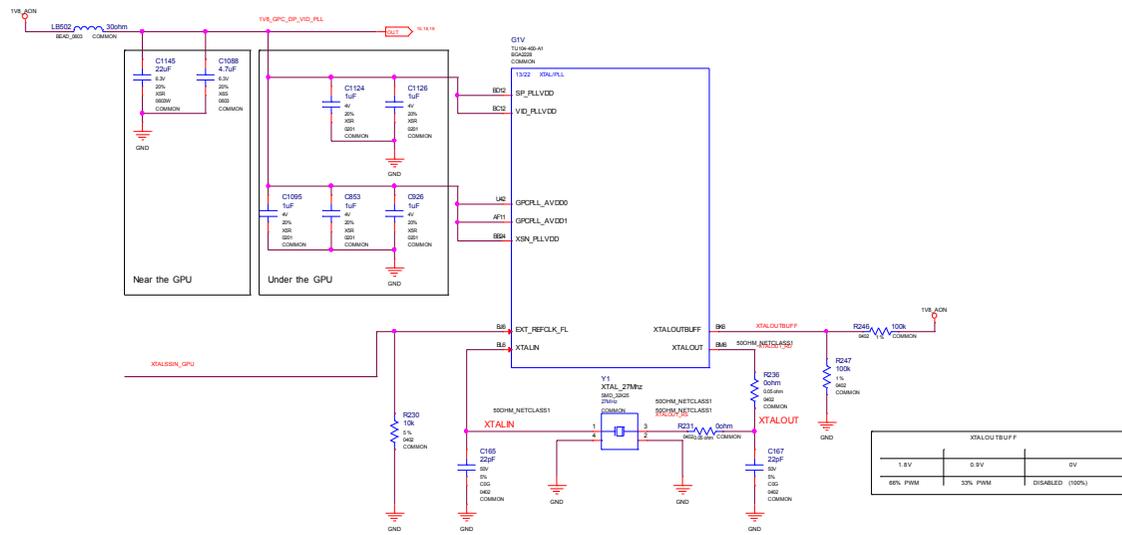
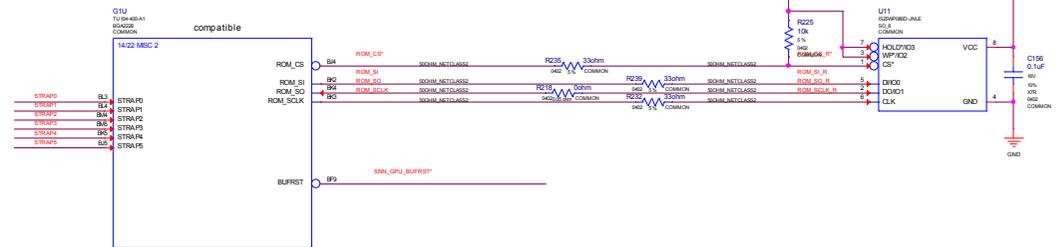
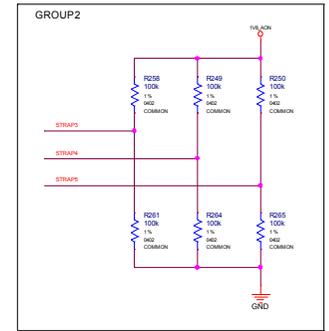
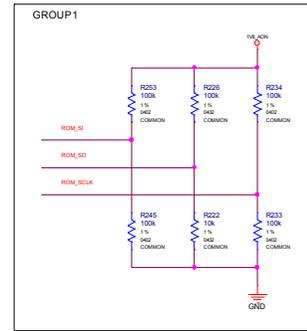
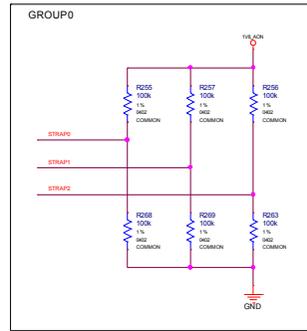
H=High :Tied to 1.8V
M=Middle:Tied to 0.9V
L=Low :Tied to 0V

1:SMB_ALT_ADDR ENABLE
0:SMB_ALT_ADDR DISABLE

1:PCIE_CFG LOW POWER
0:PCIE_CFG HIGH POWER

1:DEVID_SEL REBRAND
0:DEVID_SEL ORIGNAL

1:VGA_DEVICE ENABLE
0:VGA_DEVICE DISABLE



XTALOUTBUFF		
1.8V	0.9V	0V
80% PWM	33% PWM	DISABLED (100%)

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ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	MISC2: ROM_XTAL_STRAPS

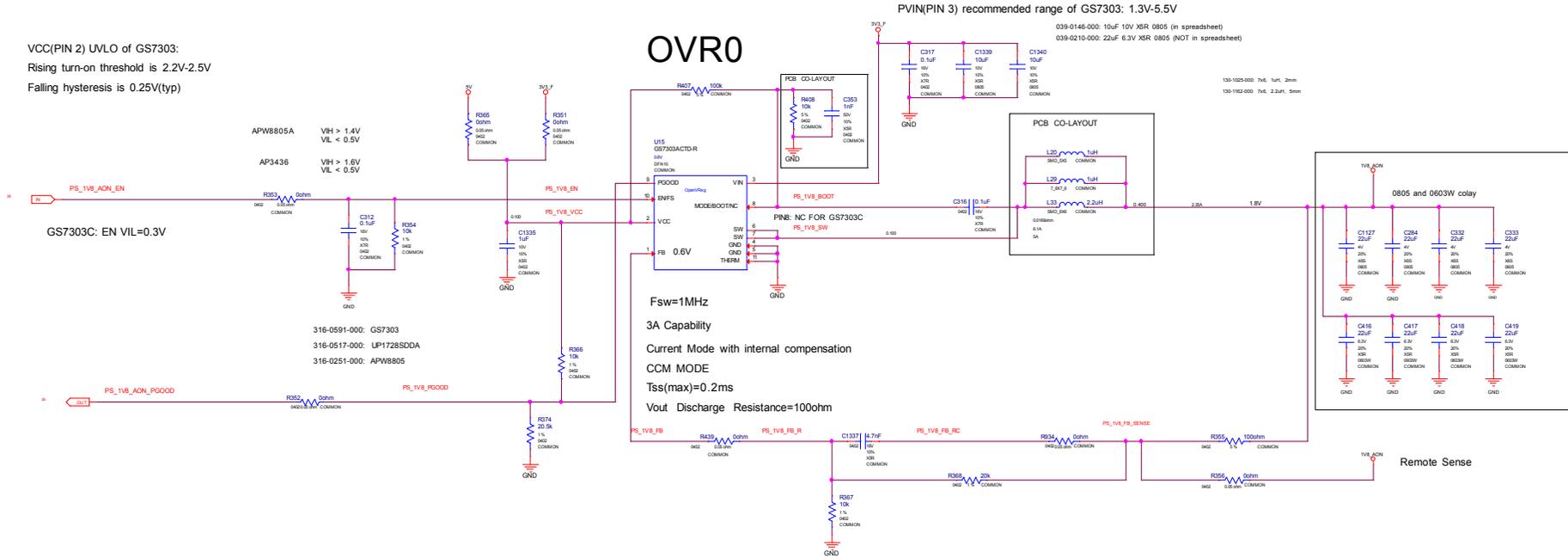
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ROM REV	A
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Use 5V as 1V8_OVR0 VCC(PIN 2), can make 1V8_AON power down later(hold more time during power down).
 And no glitch on 1V8_PGOOD.

1v8 Switcher

VCC(PIN 2) UVLO of GS7303:
 Rising turn-on threshold is 2.2V-2.5V
 Falling hysteresis is 0.25V(typ)



$$0.6V * (1 + 20K/10K) = 1.8V$$

OVR0

Fsw=1MHz
 3A Capability
 Current Mode with internal compensation
 CCM MODE
 Tss(max)=0.2ms
 Vout Discharge Resistance=100ohm

PVIN(PIN 3) recommended range of GS7303: 1.3V-5.5V

039-0146-000: 10uF 10V XSR 0805 (n spreadsheet)
 039-0210-000: 22uF 6.3V XSR 0805 (NOT in spreadsheet)

130-1020-000: 7uH 1uH 20mm
 130-1180-000: 7uH 2.2uH 20mm

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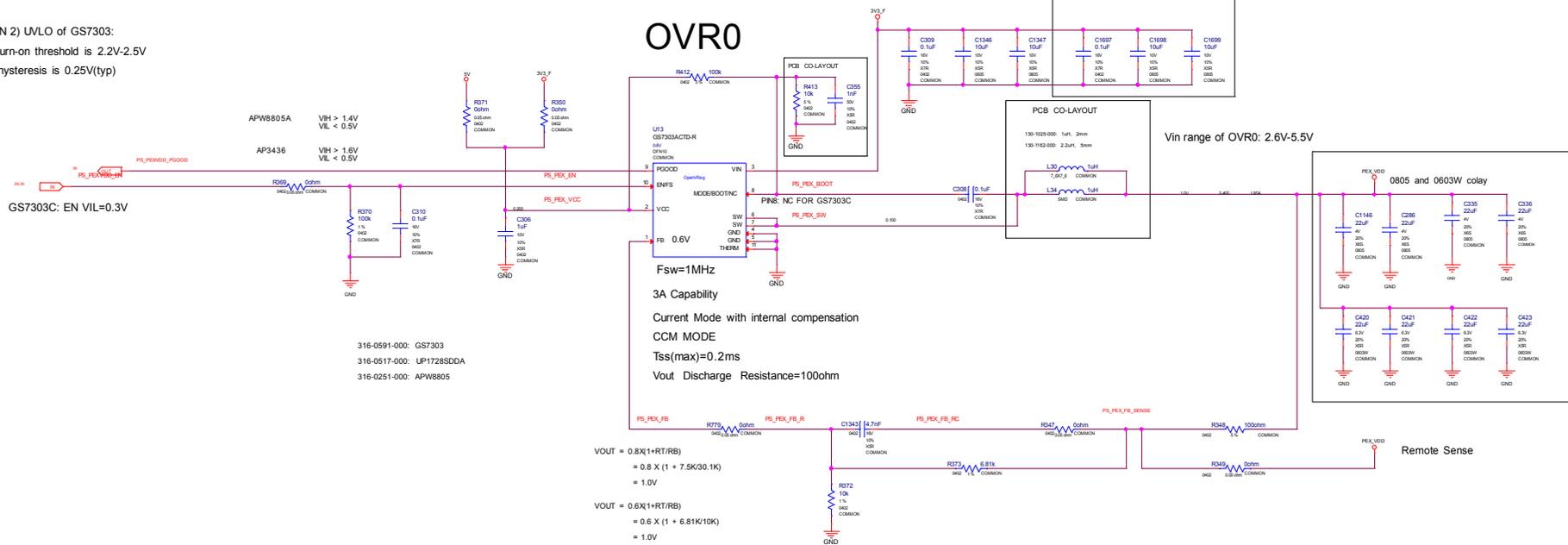
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Use 5V as PEX_VDD OVR0 VCC(PIN 2),
enable PEX_VDD OVR0 internal discharge(100ohm typ), making PEX_VDD power down faster.

PEX_VDD Switcher

ADD 3 MORE MLCC
3V3_F is Far Away From Source

VCC(PIN 2) UVLO of GS7303:
Rising turn-on threshold is 2.2V-2.5V
Falling hysteresis is 0.25V(typ)



- 316-0591-000: GS7303
- 316-0517-000: UP1728SDDA
- 316-0251-000: APW8805

$$V_{OUT} = 0.8X(1+RT/RB)$$

$$= 0.8 X (1 + 7.5K/30.1K)$$

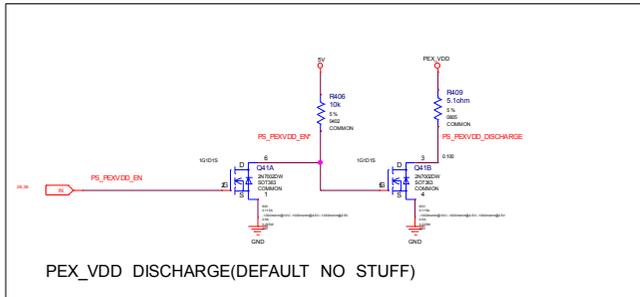
$$= 1.0V$$

$$V_{OUT} = 0.6X(1+RT/RB)$$

$$= 0.6 X (1 + 6.81K/10K)$$

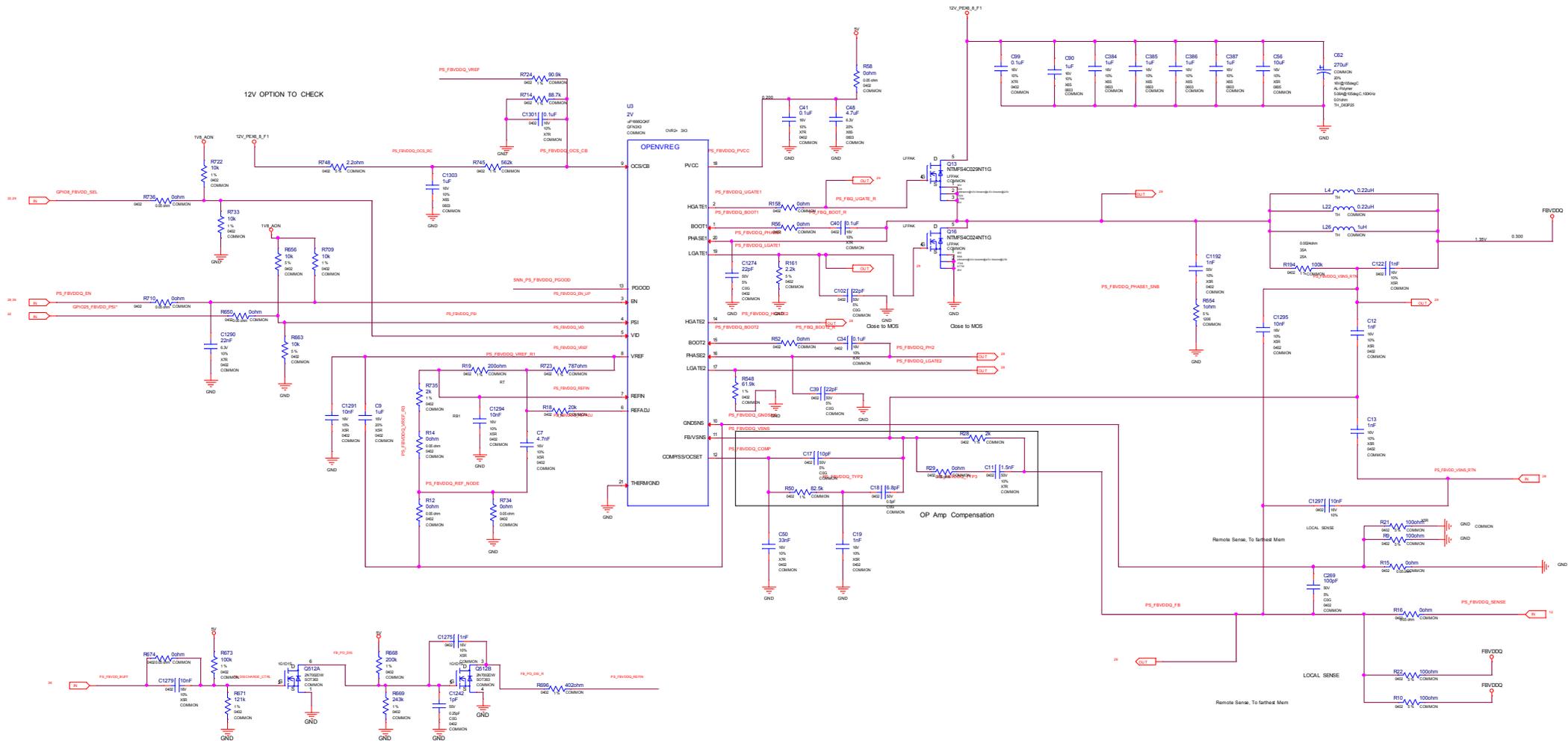
$$= 1.0V$$

$$0.6V * (1 + 6.81K/10K) = 1.008V$$



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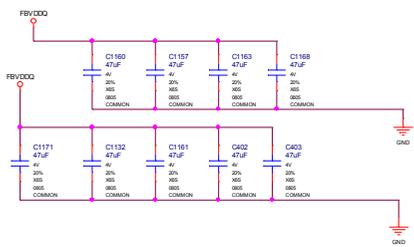
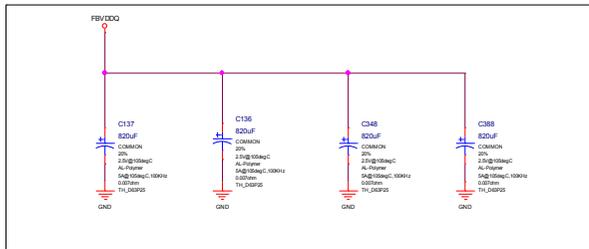
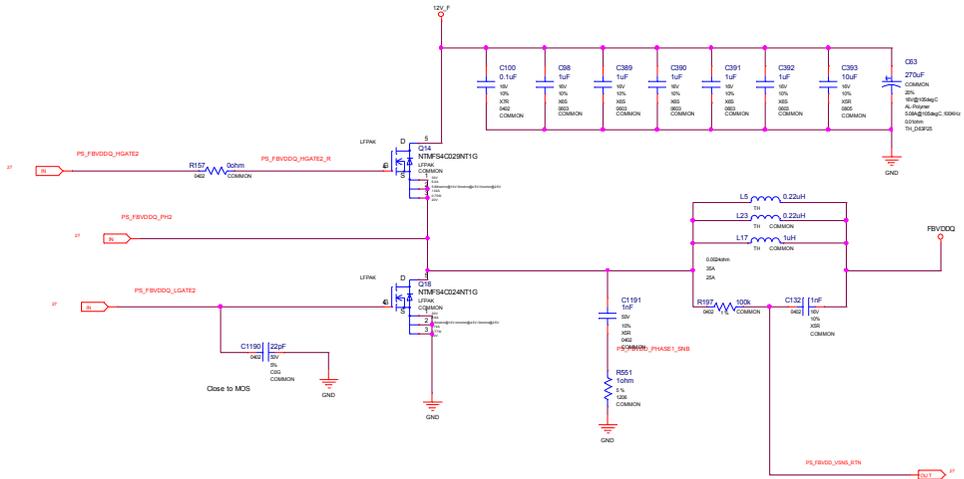
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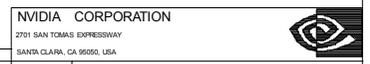
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ASSEMBLY	ASSEMBLY DESCRIPTION
FRGE DETAIL	PS: FBVDDQ

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BCW REV	A		

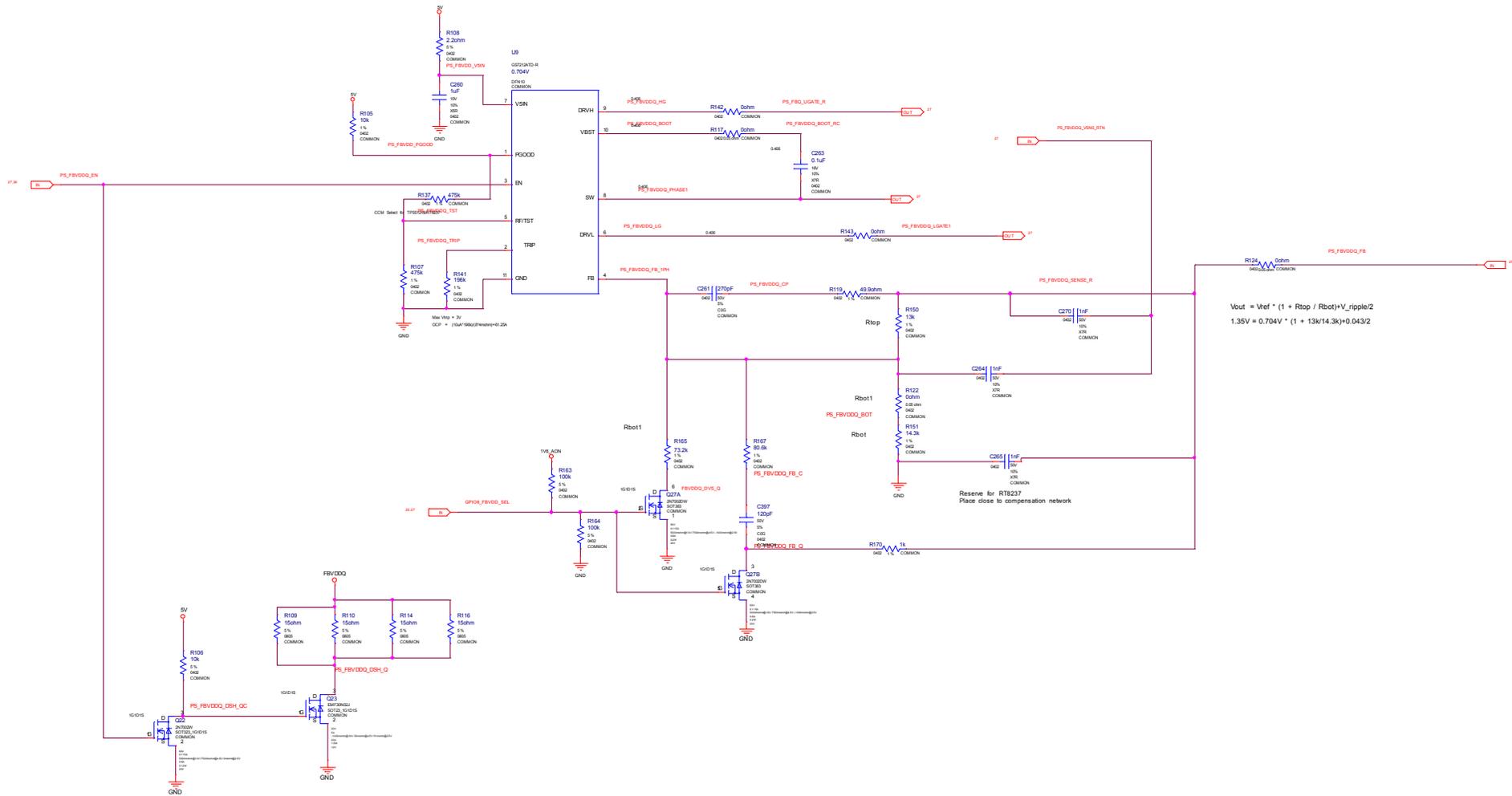


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ASSEMBLY	ASSEMBLY DESCRIPTION
PS: FBVDDQ PH2	PS: FBVDDQ PH2

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BCM REV	A	DATE	01-AUG-2019



1

2

3

4

5



600-1G166-BASE-A02

TG166-A02

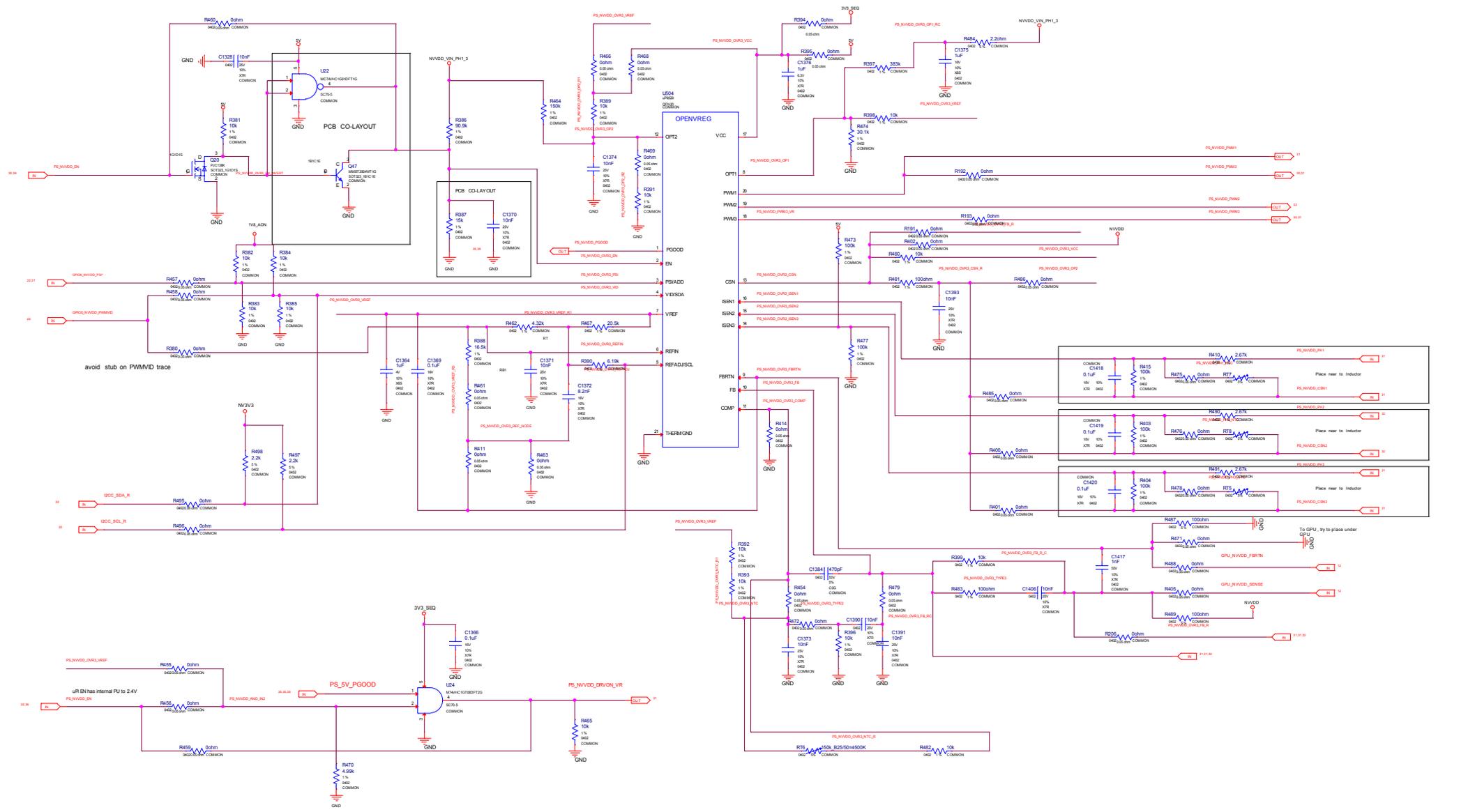
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ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE: DETAIL	PS: FBVDDQ VR option

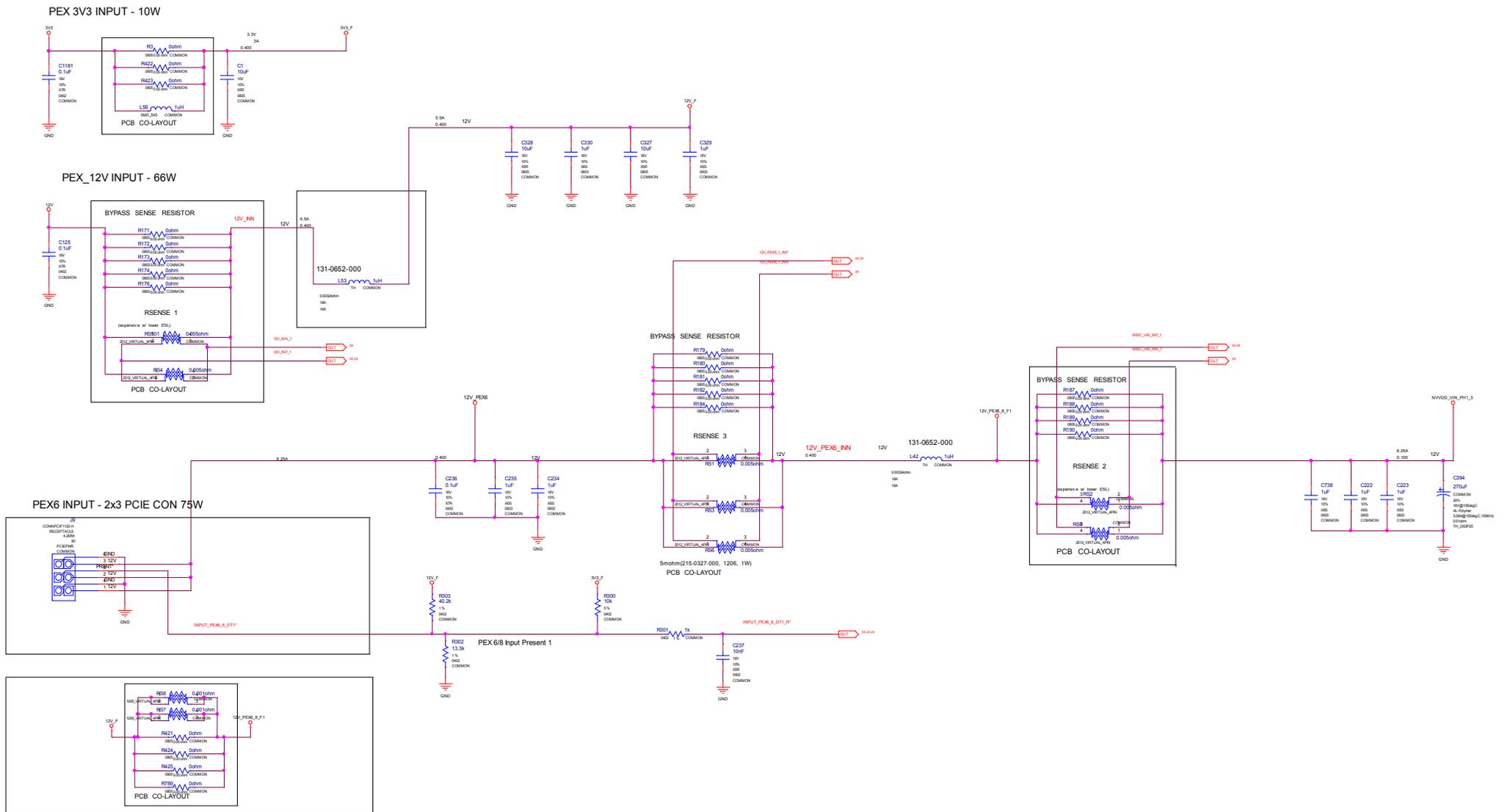


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ASSEMBLY	<ASSEMBLY_DESCRIPTION>
FRG# DETAIL	PS: NVVDD Controller

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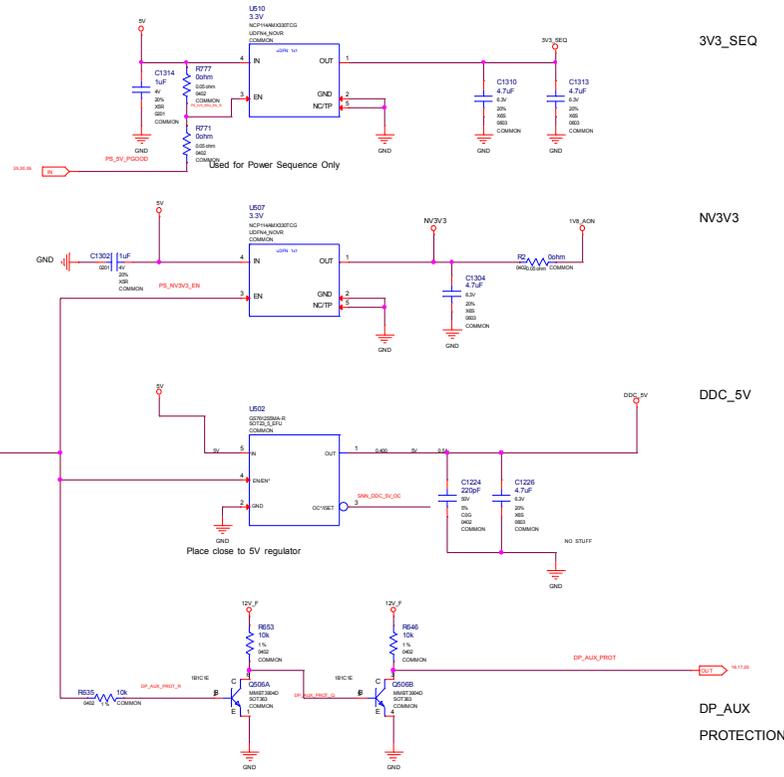
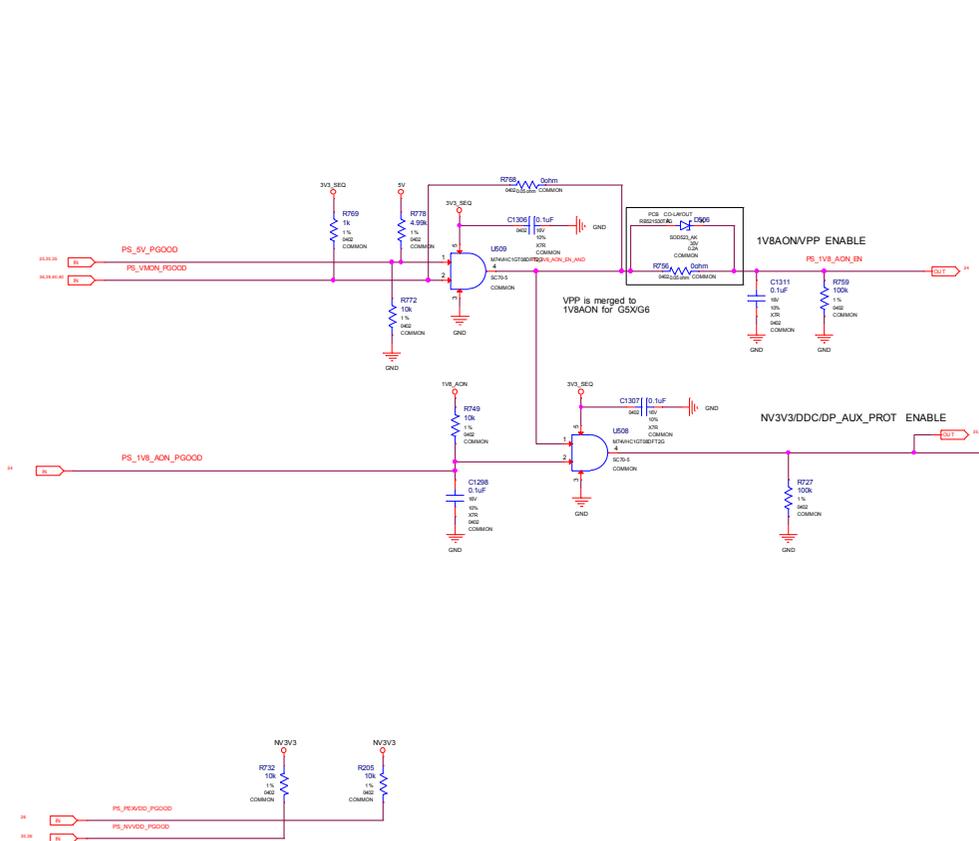




ASSEMBLY	ASSEMBLY DESCRIPTION
FRGE DETAIL	PS: Input, Filtering, and Monitoring

NVIDIA CORPORATION 2701 SAN TOMAS EXPRESSWAY SANTA CLARA, CA 95050, USA			
NV_PN PCB REV BCM REV	600-1G166-BASE-A02 1G166-A02 A		PKG# DATE

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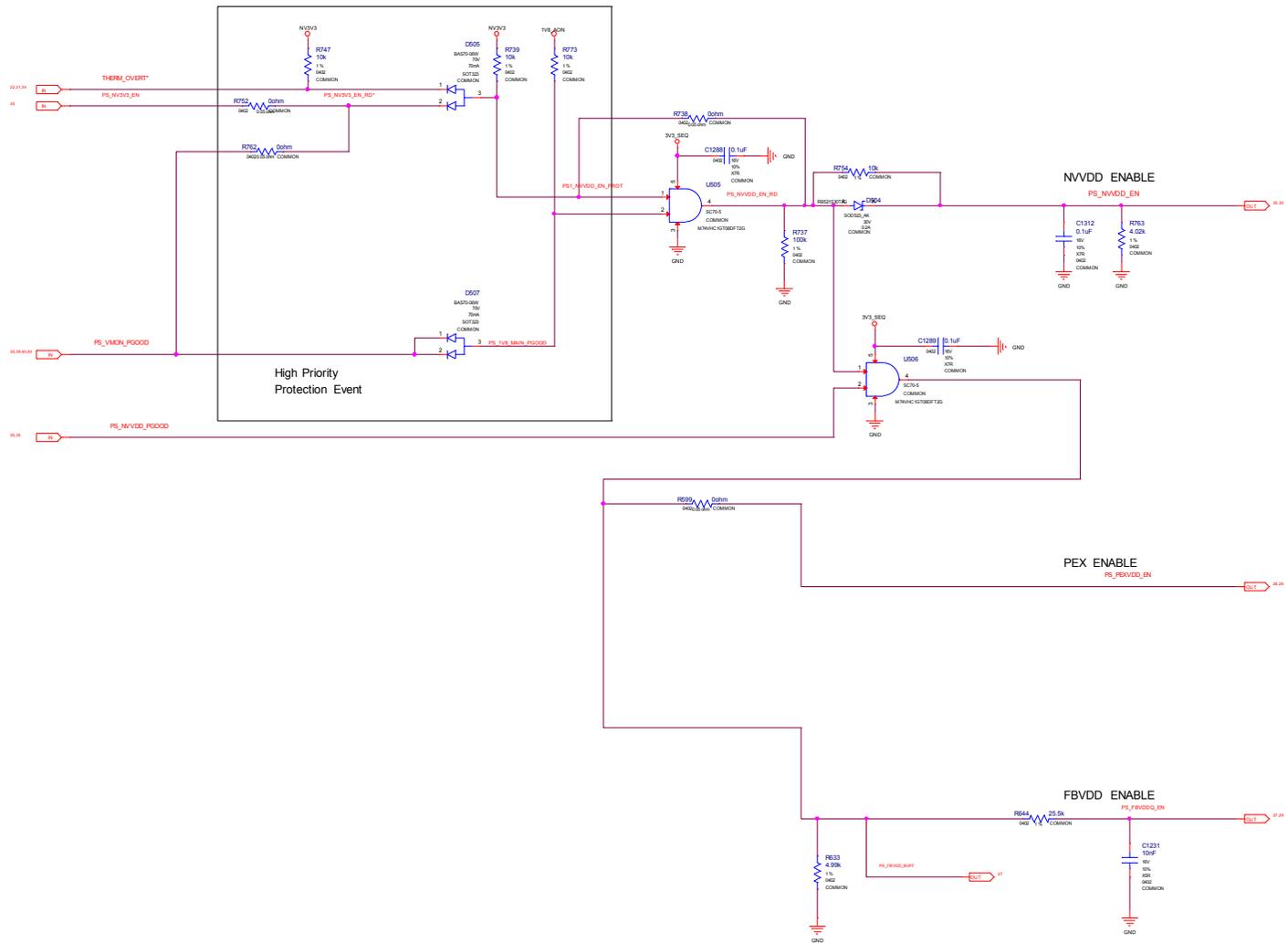


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NVIDIA CORPORATION	
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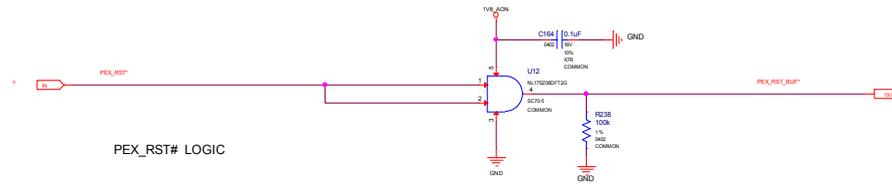
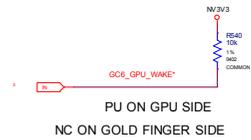


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ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	SEQ: NVVDD, PEX, FBVDDQ ENABLE

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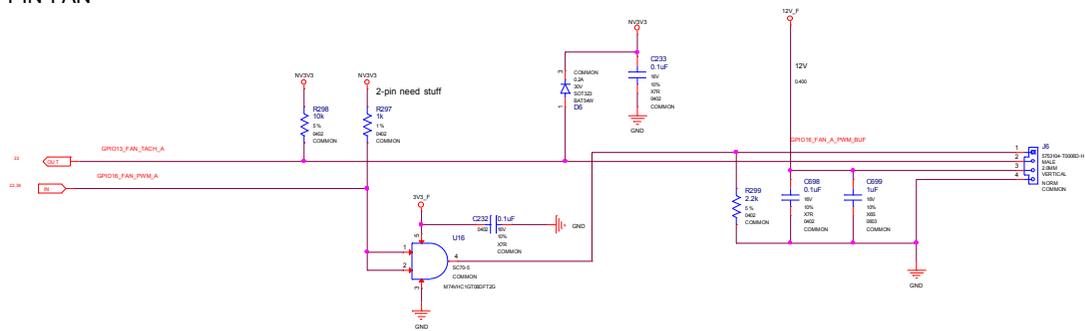


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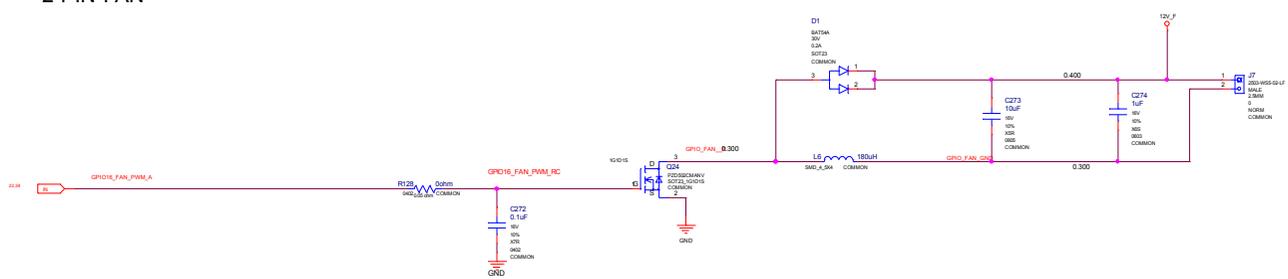
NV_PN	600-1G166-BASE-A02		
PCB REV	TG166-A02	PKGE	37 OF 41
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4-PIN FAN



2-PIN FAN

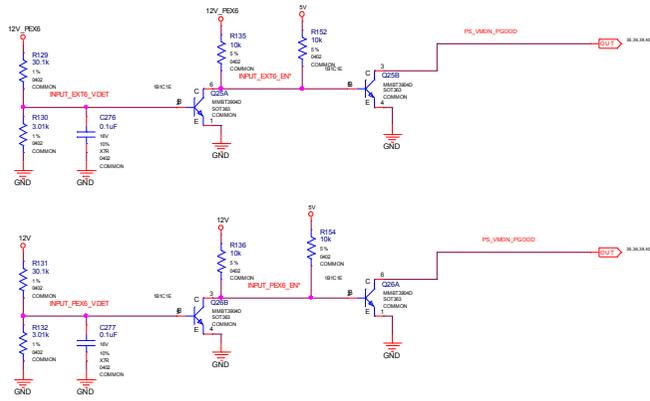


- FM 1 SW_FB
- FM 2 SW_FB
- FM 3 SW_FB
- FM 4 SW_FB
- FM 5 SW_FB
- FM 6 SW_FB
- FM 7 SW_FB
- FM 8 SW_FB

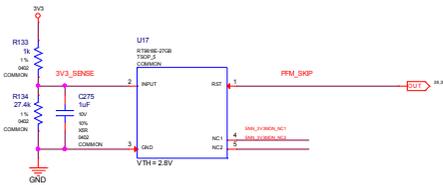
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ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	FAN

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Make the trace to PFM Sense Pin

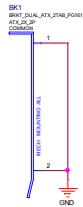


ASSEMBLY	<ASSEMBLY_DESCRIPTION>
FIGURE DETAIL	PS-Voltage Monitor

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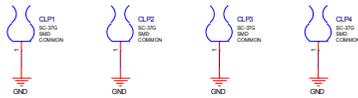
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BACK STIFFENER:



EMI CLIP:



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ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	MECH

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